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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/917,861	07/31/2001	Soon-Sung Yoo	053785-5024	9467

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EXAMINER	
LANDAU, MATTHEW C	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 11/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/917,861	Applicant(s) YOO ET AL.	
	Examiner Matthew Landau	Art Unit 2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *11-18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,19 and 20* is/are rejected.

7)☒ Claim(s) *9 and 10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 19 is rejected under 35 U.S.C. 102(b) as being anticipated by Someya et al. (US Pat. 5,528,396, hereinafter Someya).

In regards to claim 19, Figures 1 and 2 of Someya disclose a substrate SUB1; a gate line GL disposed on the substrate along a first direction, the gate line connected with a gate electrode GT of a thin film transistor TFT1; a data line DL disposed on the substrate along a second direction substantially perpendicular to the first direction, the data line connected to a source electrode SD2 (col. 6, lines 57-62) of the thin film transistor; and first and second dummy metal layers LS disposed on a semiconductor layer AS over the gate line and on opposite sides of the data line. Since there is a layer LS in each pixel, it can be considered there is a metal layer on each side of the data line. Note the term "dummy" is merely a functional label that does not structurally distinguish the claimed invention. As can be seen in Figure 2, layer LS is not electrically connected to any other elements and is therefore electrically floating.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-8 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Someya in view of Kim et al. (US Pat. 6,091,466, hereinafter Kim).

In regards to claim 1, Figures 1 and 2 of Someya disclose a substrate SUB1; a thin film transistor TFT1 disposed on the substrate, the TFT including a gate electrode GT, a source electrode SD2, and a drain electrode SD1; a gate line GL arranged in a first direction on the substrate, the gate line connected with the gate electrode of the TFT; a gate insulating layer GI disposed on the substrate and covering the gate line and the gate electrode of the TFT; an intrinsic semiconductor layer AS (col. 6, lines 52-56) disposed on the gate insulation layer; a data line DL arranged in a second direction substantially perpendicular to the first direction disposed on the semiconductor layer, the data line connected to the source electrode of the TFT; first and second dummy metal layers LS formed over the gate line and arranged on opposite sides of the data line; a passivation layer PSV2 covering the data line; the source electrode, the drain electrode, and the first and second metal layers; and a pixel electrode ITO1 contacting the drain electrode. As can be seen in Figure 4, there is a metal layer 151 in each pixel, therefore there is a metal layer on each side of the data line. Since there is a layer LS in each pixel, it can be considered there is a metal layer on each side of the data line. Note the term "dummy" is merely a functional label that does not structurally distinguish the claimed invention. As can be seen in Figure 2, layer LS is not electrically connected to any other elements and is therefore electrically floating. The difference between Someya and the claimed invention is an extrinsic semiconductor layer above the intrinsic semiconductor layer. Figure 5F of Kim discloses a TFT

with an extrinsic semiconductor layer 135 between an intrinsic semiconductor layer 133 and the source/drain electrodes 121/131. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Someya by including an extrinsic semiconductor layer as taught by Kim for the purpose of increasing the ohmic contact between the source/drain electrodes and the active layer (col. 6, lines 1-3 of Kim). Note that when the extrinsic layer is incorporated into the device of Someya as indicated above, the dummy metal layers are formed on the extrinsic layer.

In regards to claim 2, Someya discloses layers d1 and d2 of the data line DL are formed of chromium and aluminum, respectively (col. 9, lines 21 and 22 and lines 47 and 48). Someya also discloses layer LS can be formed of aluminum or chromium (col. 12, lines 35-37). Therefore, Someya discloses the first and second dummy metal layers LS are formed of a same material as the data line.

In regards to claim 3, Figure 2 of Someya discloses the first and second dummy metal layers LS are electrically isolated from the data line DL.

In regards to claim 4, Figure 1 of Someya discloses the pixel electrode ITO1 is formed of indium-tin-oxide (ITO).

In regards to claims 5, 6, and 20, Figure 2 of Someya discloses the pixel electrode ITO1 contacting a drain electrode SD1 of the thin film transistor TFT1. The difference between Someya and the claimed invention is a storage capacitor that includes a capacitor electrode, a portion of the gate line and a portion of a pixel electrode, wherein the portion of the pixel electrode contacts the capacitor electrode. Figure 5F of Kim discloses a storage capacitor that includes a capacitor electrode 151, a portion of the gate line 111 and a portion of a pixel

electrode 141, wherein the portion of the pixel electrode contacts the capacitor electrode. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Someya by including the capacitor of Kim to compensate for charge leakage (col. 6, lines 7-10 of Kim).

In regards to claim 7, Figure 1 of Someya discloses the intrinsic semiconductor layer AS extends along the gate insulation layer to cover the gate line at the intersection of the gate line and the data line.

In regards to claim 8, it is inherent in the device of Someya that the passivation layer PSV2 has a first width disposed along the first and second directions and a second width covering the intersection of the gate and data lines. Note that the claim does not require any specific relationship between the first and second widths.

Allowable Subject Matter

Claims 9 and 10 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

In regards to claim 9, the prior art of record, either singularly or in combination, does not disclose or suggest the combination of claim limitations including the second width is greater than the first width.

In regards to claim 10, the prior art of record, either singularly or in combination, does not disclose or suggest the combination of claim limitations including the passivation layer

contacts the intrinsic semiconductor layer between at least one of the first and second dummy metal layers.

Response to Arguments

Applicant's arguments filed September 8, 2004 have been fully considered but they are not persuasive.

In response to Applicant's arguments regarding claim 1 that Someya does not teach or suggest "first and second dummy metal layers on the extrinsic semiconductor layer" and that Someya merely discloses "a light shielding film LS arranged on a protection film PSV1 made of silicon oxide or silicon nitride", it is respectfully pointed out that the term "on" does necessarily imply direct contact. Therefore, although the dummy layers of Someya are above the aforementioned protection film, they can still be considered "on" the semiconductor layer below the protection film since they are indirectly connected with and above the semiconductor layer. Note that Applicant makes similar arguments regarding claim 19.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Landau whose telephone number is (571) 272-1731.

The examiner can normally be reached from 8:30 AM - 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone numbers for the organization where this application or

proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Matthew C. Landau

Examiner

November 14, 2004

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800